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Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — UNITED KINGDOM

4. Title of the invention — DIGITAL SIGNAL PROCESSING AND SIGNAL FORMAT

5. Name of your agent *(if you have one)* — D YOUNG & CO

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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Signature D Young & Co

Date 02 10 98

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12. Name and daytime telephone number of the person to contact in the United Kingdom — Richard W Pratt — 01703 634816

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2.	Patent application number *(if you know it)*	9821518.9
3.	Full name of the or of each applicant	Sony United Kingdom Limited
4.	Title of the invention	"Digital Signal Processing and Signal Format"
5.	State how the applicant*(s)* derived the right from the inventor*(s)* to be granted a patent	By virtue of assignments dated 11 November 1998 between ourselves and the overnamed inventors.
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DIGITAL SIGNAL PROCESSING AND SIGNAL FORMAT

The present invention relates to signal processors and to a signal format. In particular the invention relates to a signal format, a signal encoder for encoding a signal according to the format, a corresponding decoder, and a signal transmission system including the encoder and decoder.

It is desired to transmit packetised signals such as MPEG 2 TS (Transport Stream) packets from one location or piece of equipment to another. It is known to transmit MPEG 2 TS packets via a DVB Asynchronous Serial Interface (ASI). DVB ASI is effective for the transmission of one transport stream from point to point such as between specific items of equipment but is otherwise relatively inflexible.

According to one aspect of the invention, there is provided a transmission system in which MPEG 2 TS packets, are transmitted via an SDTI system.

Such a system provides greater flexibility than using DVB ASI. The SDTI (Serial Data Transport Interface) is defined in SMPTE 305M. SDTI transmits packets in a signal structure comprising frames of television lines. Ancillary data is carried in the horizontal blanking area of lines and data is carried in a payload area of each line. The payload area is in the active line interval. SDTI allows TS packets to be routed wherever SDI connections are available and also allows TS packets from more than one source to be transmitted. However, the carriage of TS packets over SDTI requires buffering to ensure that the packets are confined to the payload area of the SDTI and to allow multiple packets on each line for efficiency. The buffering process introduces delay and jitter (i.e. variation in the timing of the packets relative to each other) to the packets but, for accurate decoding of an MPEG 2 signal, the packets of that signal must be provided to the MPEG decoder with accurate timing relative to one another to allow correct decoding. Whilst absolute delay of packets is not a problem because it affects all packets equally, there is a need to correct jitter at or before the MPEG decoder.

Whilst the foregoing discussion describes the technical problem faced by the present invention with reference to the transmission of MPEG 2 TS packets via SDTI,

similar problems may occur in the transmission of other types of time sensitive packets over other data transmission systems.

According to another aspect of the invention, there is provided a digital signal comprising: data blocks, each data block including a header containing data relating to the block and at least one slot; each slot having a slot header relating to the slot and a data packet; the data packets containing successive parts of information from a source; a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time; and the or each subsequent slot containing a subsequent packets of the information from the said source also containing timing information defining the timing of that packet relative to the reference time.

According to another aspect of the invention, there is provided an encoder for encoding a digital signal comprising data blocks, each data block including a header containing data relating to the block and at least one slot; each slot having a slot header relating to the slot and a data packet; the data packets containing successive parts of information from a source; a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time; and the or each subsequent slot containing a subsequent packet of the information from the said source also containing timing information defining the timing of that packet relative to the reference time,

the encoder comprising a clock, and means for deriving from the clock a reference time defining the time of production of the said first packet and for providing the reference time information in the said first slot and for deriving from the clock the said timing information defining the times of production of the subsequent packages and providing the timing information in the subsequent slots as the subsequent packets are produced.

According to a further aspect of the invention, there is provided a decoder for decoding a digital signal comprising data blocks, each data block including a header containing data relating to the block and at least one slot; each slot having a slot header relating to the slot and a data packet; the data packets containing successive parts of

information from a source; a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time; and the or each subsequent slot containing a subsequent packet of the information from the said source also containing timing information defining the timing of that packet relative to the reference time

the decoder comprising a clock, means for detecting the timing information of the packets, means for initially setting the clock to the said reference time on detection of the said first packet, means for comparing the clock time with the said timing information of the subsequent packets, and means for outputting the packets at the times when the timing information of the packets equals the clock time.

By providing the timing information in the signal, the decoder is enabled to output the packets with jitter substantially reduced and preferably eliminated to allow correct decoding in for example a subsequent MPEG decoder if the packets are MPEG TS packets.. Packet jitter can corrupt the decoding. The decoder compares the timing information of each packet with an internal clock set by the reference time of the first packet and outputs the packets, to for example a buffer, when the clock time equals the packet time thus at least reducing the jitter.

In an embodiment of the invention, the blocks are payload areas in the active line intervals of SDTI signals which have ancillary data including address data in the non-active areas of the lines.

In preferred embodiments of the present invention as applied to SDTI, there is a fixed, integer, number of complete packets per SDTI line with padding (e.g. zeros) in any unused space. The slot lengths are thus fixed. The slots and packets on a particular SDTI line all have the same source and destination addresses and there is only one packet stream on that line.

For a better understanding of the present invention, reference will now be made by way of example to the accompanying drawings in which:

Figure 1 is a schematic diagram of the payload area of an SDTI line;

Figures 2a to c are schematic diagrams of MPEG 2 TS packets;

Figure 3 a schematic diagram of an SDTI payload area divided into slots and having a format in accordance with an embodiment of the present invention;

Figure 4 is a schematic diagram of the payload header structure;

Figure 5 is a schematic diagram illustrating the correction of jitter in accordance with an embodiment of the present invention;

Figure 6 is a schematic block diagram of a system, in accordance with an embodiment of the invention for transmitting MPEG 2 TS packets over an SDTI system;

Figure 7 is a schematic block diagram of an example of the timing data inserter and of the timing corrector of the system of Figure 7; and

Figures 8 and 9 are schematic block diagrams of examples of the counters of Figure 7.

For convenience, the Figures represent the data in parallel-format. In practice the data is transmitted in serial-format.

Overview

The following description describes examples of a novel signal format for carrying MPEG-2 Transport Stream packets over the SDTI (SMPTE 305M). MPEG 2 TS and SDTI are well known and will not be described herein in detail. The novel format is referred to herein as SDTI TS. SDTI uses television lines to carry data. The active line intervals are the pay load areas and contain the STDI data blocks. The non-active intervals of the lines contain ancillary data including the source and destination addresses of the data in the active line intervals. In accordance with an embodiment of the present invention, to ensure efficiency of transfer, the pay load area of each line of SDTI-TS is filled to capacity as possible with whole, fixed length, slots containing the packets from one Transport Stream. The novel format includes all information necessary to recover Transport Stream packets with a low jitter level at the SDTI-TS decoder and has the flexibility to meet a number of design requirements.

References

The following references , which are published standards, contain information relevant to the present invention.

- SMPTE 305M, Serial Data Transport Interface (SDTI).
- SMPTE RP 68, Definition of Vertical Interval Switching Point.
- ISO/IEC 13818-2: Information Technology - Generic Coding of Moving Pictures and Associated Audio Information: Video, (MPEG-2).
- ISO/IEC 13818-2: Information Technology - Generic Coding of Moving Pictures and Associated Audio Information: Systems, (MPEG-2).
- DVB: Interfaces for CATV/SMATV Headends and Similar Professional Equipment; Asynchronous Serial Interface (ASI).
- SMPTE 259M, 10-bit 4:2:2 Component and 4fsc NTSC Composite Digital Signals/Serial Interface.
- SMPTE 291 M, Ancillary Data Packet and Space Formatting.
- SMPTE RP168, Definition of Vertical Interval Switching Point.

Background

The currently established interface for the carriage of MPEG-2 Transport Stream (TS) packets is the DVB ASI which places packets within a small tolerance of the position required to ensure minimal impact on the decoder buffer. However, ASI cannot easily carry more than one TS, neither can ASI be supported by commonly available SDI based equipment. It is useful as a specialised point-to-point interface between specific items of equipment.

Illustrative examples of the present invention

One aspect of the present invention proposes the carriage of MPEG2 TS packets over the SDTI. This allows a more general approach to connectivity by allowing TS packets to be routed wherever SDI connections are available. However, the carriage of TS packets over the SDTI requires buffering to ensure that packets are confined to the payload area of the SDTI and to allow multiple TS packets on each line for efficiency. The result of this buffering process is to introduce both a delay and

jitter to the packet stream. The delay is not a problem which concerns the present invention. The examples of the present invention described herein allow the packet jitter to be reduced to insignificant levels. As a benchmark, the present embodiments allow a DVB-ASI input to be carried through SDTI-TS and decoded to create a new DVB-ASI signal with minimum additional jitter.

The SDTI-TS can also operate directly from other interface points as required.

SDTI PARAMETERS

SMPTE305M specifies the SDTI for bit rates of 270Mbps and 360Mbps and examples of the invention may operate on both bit rates and on higher frequency bit rates.

The examples of SDTI-TS described herein use the fixed block size mode of the SDTI with one block per line. The format of each fixed length block is shown in Figure 1. The block is either 1438 or 1918 bytes long including a ten bit TYPE word as described hereinafter. The block typically includes an additional 2 bytes of error correction CRC for a total of 1440 or 1920 bytes as shown in Figure 1.

TYPE WORD

The data block has a block type word.

For 270Mbps SDTI, the Block Type value is "0lh" which specifies a block size of 1438 words per line (including the Type value).

For 360Mbps SDTI, the Block Type value is "09h" which specifies a block size of 1918 words per line (including the Type value).

The SDTI Data Type word has the value "253h" as pre-defined by table 2 of SMPTE 305M and is shown as TYPE at the left hand side of Figure 1.

The input format is 8 bit data entered into bits b7 -b0 of a 10 bit word. Bit b8 of the 10 bit word is the even parity of bits b7-b0 and bit b9 is the complement of bit b8.

The optional FEC (Forward Error Correction) may be added to the block to give added data security. Whether FEC is added or not, bits b7 and b6 of the Block Type word are set according to SMPTE 305M.

The present examples of the invention do not use the Data Extension facility of SMPTE 305M. It is recommended to avoid use of the SDI switching lines as defined in SMPTE- RP 168

MPEG-2 TRANSPORT STREAMS

As shown in Figure 2a, MPEG-2 TS (Transport Stream) packets are 188 bytes in length. As shown in Figure 2b if DVB Forward Error Correction (FEC) is added, then the packet length is 204 bytes. The MPEG-2 TS FEC is interleaved across packets and designed for serious data loss through transmission errors which may be bursty. Whilst in extreme cases SDTI can create occasional errors, the MPEG-TS FEC is unsuitable for correcting SDTI errors due to the interleave length and this FEC will not exist if the packets carried are only 188 bytes in length. Consequently, the SDTI-TS format of am embodiment of the invention includes an optional FEC to correct for any errors which may occur through the SDTI link.

PAYLOAD FORMAT

In accordance with embodiments of the invention, the MPEG-2 TS packets are wholly contained in an SDTI fixed block placed in a TS Payload format an example of which is described as follows with reference to Figure 3.

The illustrative TS Payload format has a 2 layer structure as indicated in Figure 3. The payload has a TS Payload header defining parameters which apply to the whole payload line, and a fixed number of TS Slots into which the MPEG2 TS packets are placed. Each TS Slot has a slot header which defines parameters associated with the TS packet in the slot, followed by the TS packet itself and terminated by an optional SDTI RS-FEC of 6 bytes.

TS Payload Structure

The Type word of the TS Payload is pre-defined by SMPTE 305M to have the 10 bit word value of "253h, which is the type word at the left hand side of figure 1.

The bit assignments of the Slot Count, Channel Handle and Continuity Count words are shown in Figure 4.

TS Payload Slot Count

The Slot Count is an 8 bit word which defines the number of TS Slots for this payload line. The number of TS Slots has a lower value of 1 and an upper value defined by the payload length.

In the case of 270Mbps SDTI, the maximum number of TS Slots is 6. In the case of 360Mbps SDTI, the maximum number of TS Slots is 8. Higher SDTI rates can support appropriately higher numbers of TS Slots in the payload area.

In the present embodiments of the invention, data space between the last TS Payload Slot and the SDTI CRC words is not used for any other purpose or application.

Lower values of payload slot count tend to reduce the codec delay. Further information on this topic is given herein below.

TS Payload Channel Handle

The Channel Handle is a 16 bit word organised as two 8 bit words with the most significant word first. This word is used to distinguish between TS Payload lines having the same SDTI source and destination header addresses but representing different channels of TS transmission.

In the present embodiments the Channel Handle value is set to "0000h" but other values may be chosen.

TS Payload Continuity Count

The "Continuity Count" is a modulo 65536 count which increments by 1 for every TS Payload line having the same SDTI Source and Destination addresses and the same Channel Handle value. The purpose of this count is to provide detection of signal path switching.

TS Slot Structure

In the present embodiments every TS Slot is 216 words in length and TS Slots are arranged in continuous order immediately following the TS payload header.

A TS Slot contains information in the following sequence:

a TS Slot header of 2 word length,

a coarse 2.25MHz count value of 2 words in length,

a fine count value of a multiple of 2.25MHz which is one word in length.

a 188 byte TS Packet,

a 16 byte space for the optional MPEG-2 TS FEC,

a 6 byte space for the optional SDTI-TS FEC and

a 2 byte null data space.

TS Slot Header

The TS Slot header is an 8 bit word with bits b7-b0 defined as follows:

Bit b7 defines whether the TS Slot has an active SDTI FEC.

b7 is "0" if the SDTI FEC is not active and is " 1 " if the SDTI FEC is active.

Bits b6-b3 are reserved but not defined.

Bit b2 is a TS discontinuity flag. If the TS packet in this TS slot is not related to the previous TS packet, then b2 shall be set to "1", else it shall be set to "0". A discontinuous TS packet (i.e. b2='1') also indicates that this is the first packet in a new TS packet sequence.

Bits b1 I and b0 form a code which define the TS packet type as follows:

b1	b2	TS Type
0	0	188 byte TS packet with no 16 byte FEC.
0	1	Reserved but not defined.
1	0	204 byte TS packet with an inactive 16 byte FEC
1	1	204 byte TS packet with an active 16 byte FEC.

TS Slot 2.25MHz Count

The 2.25MHz count value is derived from a modulo 65536 counter at the SDTI-TS encoding point and defines the coarse timing of the TS packet for the decoder to be able to output the TS packet at the correct time relative to the previous TS packet. This coarse timing is used in conjunction with the next word, the TS Slot sub count which contains a fine timing derived from a clock at an integer multiple of 2.25MHz to provide a clock with a reference timing close to that of the TS Program Clock Reference (PCR). The coarse and fine timing are preferably derived from the same master clock which is for example the PRC clock operating at 27 MHz.

It is not required for the 2.25MHz counter to match the period of the PCR of 27 hours. The 2.25MHz counter only needs a sufficient cycle period guaranteed to be longer than the maximum period between TS packets. The 2.25MHz cycle period is approximately 30msecs.

The 2.25MHz count increments by 1 for every 12 increments of the PCR.

TS Slot Sub Count

In the case of 270Mbps SDTI, the sub count is clocked by a 27MHz clock (which is at the same rate as the PCR) and counts over the range 0 to 11.

In the case of 360Mbps SDTI, the sub count is clocked by a 36MHz clock (which is at a higher rate than the PCR) and counts over the range 0 to 15.

The number of bits available for the Sub Count value allows SDI word (parallel) clock rates up to 576MHz.

How the TS Slot counts can be used for output timing control is described herein below.

TS Packet Data

The 204 byte space for the TS packet is a fixed allocation. The contents of this space are filled with 188 byte or 204 byte TS packet data as defined by bits b1 and b0 of the TS slot header word.

In the cases of 188 byte TS packets and of 204 byte TS packets with inactive TS FEC, the 16 byte TS FEC space is null filled.

TS Slot RS FEC

The FEC is applied over the 214 bytes of the TS slot from the 2.25MHz count word to the last word of the FEC.

If the TS slot header word FEC valid bit (b7) is set to "0", then all 6 words of the FEC are set to "00h".

The FEC is a Reed-Solomon, R-S(214, 208, T=3) shortened code from the original R-S(255, 249, T=3) code.

The R-S code generator polynomial is:

$$R\text{-}S(x) = (x \oplus \alpha^0).(x \oplus \alpha^1).(x \oplus \alpha^2).(x \oplus \alpha^3).(x \oplus \alpha^4).(x \oplus \alpha^5)$$

where α is defined by the Galois Field GF(256) generator polynomial:

$$GF(x) = x^8 \oplus x^4 \oplus x^3 \oplus x^2 \oplus 1.$$

TS Slot Null Space

The TS slot ends with 2 words of zero filled null space.

USING THE TS SLOT TIMING DATA

Figure 5 illustrates the SDTI-TS coding process from the MPEG-2 TS packet stream input to output through the SDTI-TS format

The combination of the TS Slot 2.25MHz count and the sub count values defines a count value with a resolution at least as high as the PCR and with a period before repetition of approximately 30msecs. On reception of the first TS packet in a sequence, the decoder may output the packet whenever it is ready and, at the same time, sets an internal counter running at the SDTI word rate (27/36MHz) to the TS slot count value. This counter counts in the same manner as defined for the 2.25MHz count and sub count. Thereafter, for all remaining packets, the decoder outputs a packet when the decoder counter equals the counter stored in the TS slot count thus guaranteeing the integrity of the output TS packet timing. In the case of 270Mbps

SDTI, the count value clocks at the same rate as the TS packet PCR and should result in no timing jitter. In the case of 360Mbps SDTI, the count increments by 4 for every 3 increments of the TS packet PCR, therefore, resulting in + or - 1 PCR clock jitter. This value is well within the MPEG-2 defined limits.

SYSTEM DELAY CONSIDERATIONS

The pay load area of each SDTI line is packed with as many complete slots and thus TS packets as possible. In the present embodiments the slots are of fixed length and the SDTI payload area contains only complete slots Spare space in a payload area is filled with zeros. This ensures that the waste of SDTI lines is minimised and thus the maximum number of lines are available for the transfer of other data.

The following examples are based on 270Mbps SDTI-TS.

At a bit rate of 4Mbps, approximately 15 lines per frame (525/60) are used for the carriage of MPEG-2 TS packets and the codec delay is just over 2msec.

At a bit rate of 50Mbps, approximately 185 lines per frame (525/60) are used for the carriage of MPEG-2 TS packets and the codec delay is thus reduced to around 200uec.

To a first approximation, the codec delay is inversely proportional to the bit rate. Thus at low bit rates, delay can only be reduced by reducing the number of TS packets per line and thus occupying proportionately more SDTI lines. If the 4Mbps example above occupied only 1 TS packet per line, then the delay would be reduced to approximately 400 usec.

Example of an SDTI TS system

Referring to Figure 6 there is shown an example of an SDTI TS system. The system comprises a data source 1. The data source 1 includes an MPEG2 encoder 2 which is known and which produces known MPEG 2 TS packets. The packets may or may not include the FEC data, as shown in Figures 2a to 2c. The packets are outputted from the MPEG encoder with the correct relative timing: i.e. they are jitter-free. A timing data inserter 4 of the source 1 (and described in more detail with reference to Figures 7 and 8) inserts the coarse and fine timing data into a header. The timing data

defines the correct timing of the packets relative to a reference time. The MPEG2 TS packets with the timing data are fed to the SDTI 6. The SDTI 6 also receives packets and other data from other sources 3 and 5. The other sources may or may not be the same as source 1. The SDTI routes the data from the sources 1, 3 and 5 in known manner to respective corresponding destinations 11, 13 and 15. For that purpose one SDTI line has a source address and a destination address in its ancillary data and carries only data from the addressed source to the addressed destination. As described above the MPEG2 TS packets are buffered in the SDTI so that they incur jitter. At the destination 11 the packets from source 1 are subject to timing correction in corrector 8 before delivery to an MPEG decoder with the correct timing. An example of the corrector 11 is described with reference to Figures 7 and 8.

The SDTI assembles the MPEG2 TS packets into the slots shown in Figure 3 adding the slot header data to the timing data and adding the block header data, as also shown in Figure 3, to the block. The SDTI also adds the 6 byte FEC , the zeros for the null space and the optional SDTI CRC. The SDTI also determines when a packet is the first packet of a new packet sequence and sets the bit b2 of the TS discontinuity flag to '1'.

Referring to Figure 7, an example of the timing data inserter comprises a 27MHz clock 40 which clocks a counter 42 to produce the timing data. The clock 40 may be synchronised to, or be, the Program Clock Reference PCR. An example of the counter is shown in Figure 8. The counter comprises a Modulo 12 counter 80 clocked at 27MHz which produces the fine timing data and which produces a 2.25MHz clock for clocking a Modulo 65536 counter 82 which produces the coarse timing data. The counters 80 and 82 are free running. A latch 44 temporarily stores the fine and coarse counts. Upon receiving a packet start signal it feeds the current counts to a multiplexer 46 which inserts the timing data into the bit stream at the start of the packet. The first packet of a packet sequence is allotted whatever arbitrary time is indicated by the counter 42 at the moment of its production. That time is a reference time for the subsequent packets of the sequence. The counter 42 sequences through its counts with a period of $65536/(2.25 * 10^{6})$ seconds or about 30 ms.

At the destination, an example of the corrector 8 comprises a demultiplexer 84 which detects the slot header and determines therefrom whether a packet is the first in a sequence as indicated by the discontinuity flag (b2=1) and the fine and coarse timing data. The demultiplexer separates the MPEG2 TS packet from the slot header and feeds the packet to a FIFO buffer 96. The FIFO buffer 96 stores one SDTI block of packets. The packets are on average clocked into and out of the FIFO at the same rate e.g. 270 M bits per second as they are originally produced at the source 1. However, the packets may be input irregularly but are output continuously with correct timing. The demultiplexer feeds the timing data to a comparator 88 via another FIFO 86 and directly to a gate 94. If the packet is a first packet, the discontinuity flag b2=1 enables the gate 94 to load the timing data, which represents the reference time, into the counter 90, thereby setting the counter to the reference time.

The counter 90 an example of which is shown in Figure 9 comprises a modulo 12 counter 92 and a modulo 65536 counter 94 arranged identically to the corresponding counter 80 and 82 of Figure 8 and counting a 27MHz clock provided by the SDTI. The clock provided by the SDTI is synchronous in known manner with the source clock 40. The counters 92 and 94 differ from the counters 80 and 82 in that they can be preloaded with the reference count. Once loaded the counters 92 and 94 are free- running in the same way as the counters 80 and 82 and are thus in delayed synchronism with them.

The comparator 88 compares the timing data from the demultiplexer with the timing data from the counter 90. When the compared timing data are equal, the comparator enables the FIFO 96 to output a packet with the correct timing.

The packets and the timing data are separated by the demultiplexer 84 and fed into the FIFOs 86 and 96. The FIFOs contain corresponding sequences of packets and timing data. As the packets are moved through the FIFO 96 to its output, so are the corresponding timing data moved through the FIFO 86 to maintain correspondence wiht the packets in the FIFO 96. After each item of timing data reaches the output of the FIFO 86 that item is cleared from the FIFO. Each item of timing data at the output

of the FIFO 86 is compared with the count in the counter 90 and when the count represented by the timing data equals the count in the counter, a read out enable signal causes the FIFO 96 to start reading out the corresponding packet which accordingly has the correcr timing. The enable signal also clears the timing data from the output of the FIFO 86 and moves the next item of timing data to the output to be compared wiht the count in the counter 90.

CLAIMS

1. An encoder for encoding a digital signal comprising data blocks, each data block including a header containing data relating to the block and a plurality of slots; each slot having a slot header relating to the slot and a data packet; the data packets containing successive parts of information from a source; a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time; and the or each subsequent slot containing a subsequent packet of the information from the said source also containing timing information defining the timing of that packet relative to the reference time,

the encoder comprising a clock, and means for deriving from the clock a reference time defining the time of production of the said first packet and for providing the reference time information in the said first slot and for deriving from the clock the said timing information defining the times of production of the subsequent packages and providing the timing information in the subsequent slots as the subsequent packages are produced.

2. An encoder according to claim 1, wherein the timing information comprises coarse and fine timing information.

3. An encoder according to claim 2, wherein the clock comprises an input for receiving a clock signal, a modulo n counter which counts the clock signal and divides the clock signal frequency by n to produce the fine time information and a modulo m counter which counts the frequency divided clock signal produced by the modulo n counter, to produce the coarse time information, wherein m is much greater than n.

4. An encoder according to claim 3, wherein the clock signal frequency is 27MHz, n is 12 and m is 65536.

5. An encoder according to claim 1, 2, 3 or 4, comprising a multiplexer for inserting the time information in the slots.

6. An encoder according to anyone of claims 1 to 5, further comprising means for inserting into the slot header a flag indicating whether the slot contains a said first packet.

7. A decoder for decoding a digital signal comprising data blocks, each data block including a header containing data relating to the block and a plurality of slots; each slot having a slot header relating to the slot and a data packet; the data packets containing successive parts of information from a source; a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time; and the or each subsequent slot containing a subsequent packet of the information from the said source also containing timing information defining the timing of that packet relative to the reference time

the decoder comprising a clock, means for detecting the timing information of the packets, means for initially setting the clock to the said reference time on detection of the said first packet, means for comparing the clock time with the said timing information of the subsequent packets, and means for outputting the packets at the times when the timing information of the packets equals the clock time.

8. A decoder according to claim 7, wherein the timing information comprises coarse and fine timing information.

9. A decoder according to claim 8, wherein the clock comprises an input for receiving a clock signal, a modulo n counter which counts the clock signal and divides the clock signal frequency by n to produce the fine time information and a modulo m counter which counts the frequency divided clock signal produced by the modulo n counter, to produce the coarse time information, wherein m is much greater than n.

10. A decoder according to claim 9, wherein the clock signal frequency is 27MHz, n is 12 and m is 65536.

11. A decoder according to claim 7, 8, 9 or 10, for use with a signal the slot header of which contains a flag indicating whether the slot contains a said first packet, the decoder comprising a demultiplexer for separating the flag and the packet, and means responsive to the flag for setting the clock to the reference time if the flag indicates a first packet.

12. A decoder according to anyone of claims 7 to 11, wherein the outputting means comprises a FIFO buffer.

13. A transmission system in which MPEG 2 TS packets, are transmitted via an SDTI system.

14. A digital signal comprising: data blocks, each data block including a header containing data relating to the block and at least one slot ; each slot having a slot header relating to the slot and a data packet; the data packets containing successive parts of information from a source; a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time; and the or each subsequent slot containing a subsequent packets of the information from the said source also containing timing information defining the timing of that packet relative to the reference time.

15. A signal according to claim 14, wherein the timing information comprises coarse timing information and fine timing information.

16. A signal according to claim 15, wherein the coarse and fine timing information are represented by separate words in the slot header.

17. A signal according to claim 14, 15, or 16, wherein the slot header includes data indicating whether or not the packet is a first packet.

18. A signal according to claim 14, 15, 16 or 17, wherein the slot header includes data indicating packet type.

19. A signal according to claim 18, wherein the data indicating packet type indicates one or both of: (i) packet length; and (ii) whether the packet includes active error correction data.

20. A signal according to claim 19, wherein each packet includes error correction data.

21. A signal according to any one of claims 14 to 20, wherein the slot header includes data indicating whether or not the slot contains error correction data.

22. A signal according to claim 21, wherein each slot contains error correction data.

23. A signal according to any one of claims 14 to 22, wherein the slots of each block are of fixed length and have predetermined positions in the block.

24. A signal according toany ones of claims 14 to 23, wherein the blocks and block headers conform to SDTI.

25. A signal according to anyone of claims 14 to 24, wherein the said packets are MPEG 2 TS packets.

ABSTRACT

DIGITAL SIGNAL PROCESSING AND SIGNAL FORMAT

A digital signal comprises. data blocks, each data block including a header containing data relating to the block and a plurality of slots. Each slot has a slot header relating to the slot and a data packet. The data packets contain successive parts of information from a source. A first slot contains a first packet containing a first part of the said information from the source also contains a reference time. The or each subsequent slot contains a subsequent packet of the information from the said source also timing information defining the timing of that packet relative to the reference time.

An encoder which encodes such a signal is provided. The corresponding decoder is enabled to correctly output the packets to allow correct decoding. Absolute delay of the packets has no effect on decoding. Jitter (i.e. variation in the timing of the packets relative to each other) corrupts the decoding. The decoder compares the timing information of each packet with an internal clock set by the reference time of the first packet and outputs the packets when the clock time equals the packet time thus at least reducing the jitter. In a transmission system the packets are MPEG 2 TS packets, which are transmitted via an SDTI system.

(*Figure 3*)

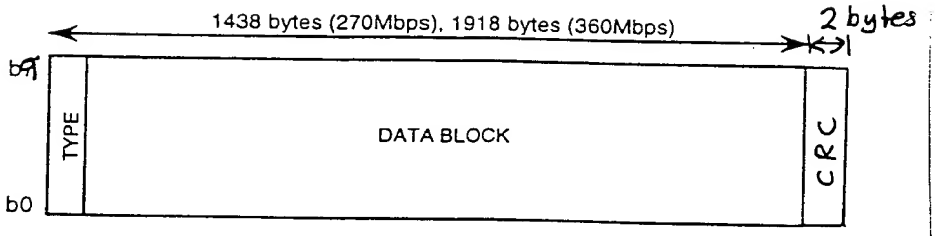

Figure 1: Format of the SDTI-TS Fixed Block

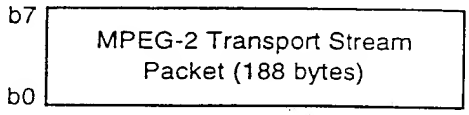

Figure 2a: MPEG-2 Transport Stream Packet

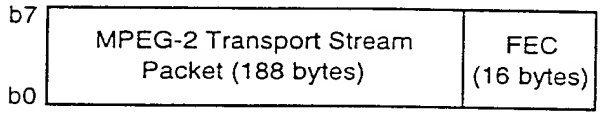

Figure 2b: MPEG-2 Transport Stream Packet with Active 16 byte FEC

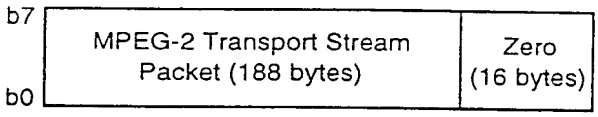

Figure 2c: MPEG-2 Transport Stream Packet with Null FEC Space

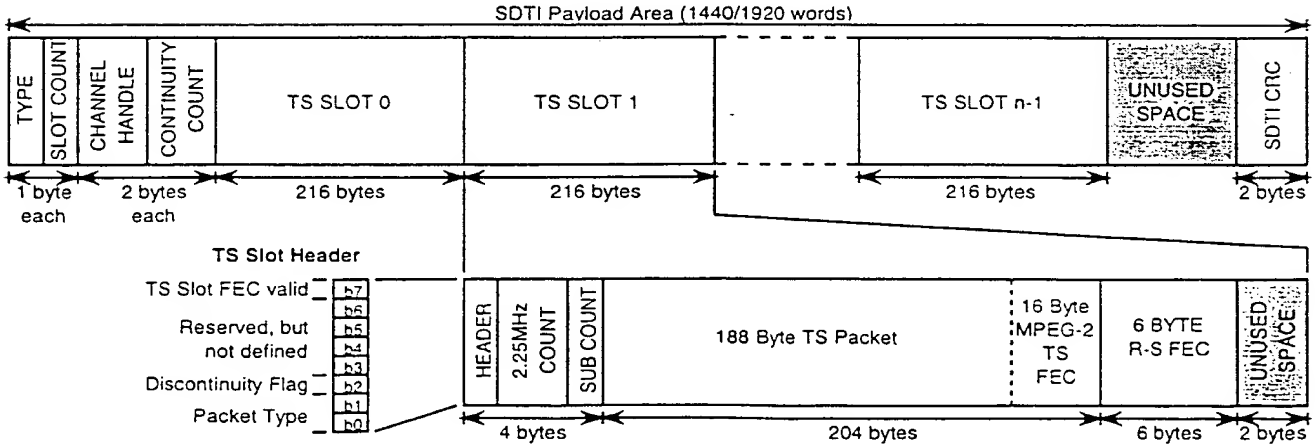

Figure 3: TS Payload Structure

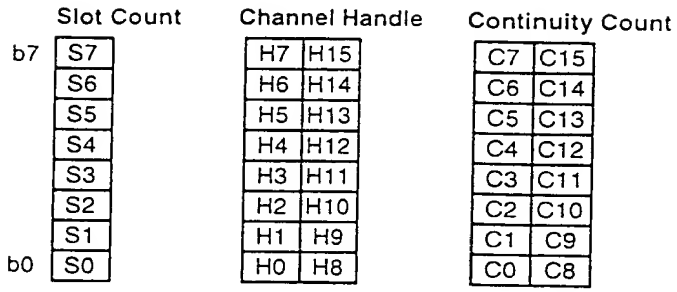

Figure 4: Payload Header Structure

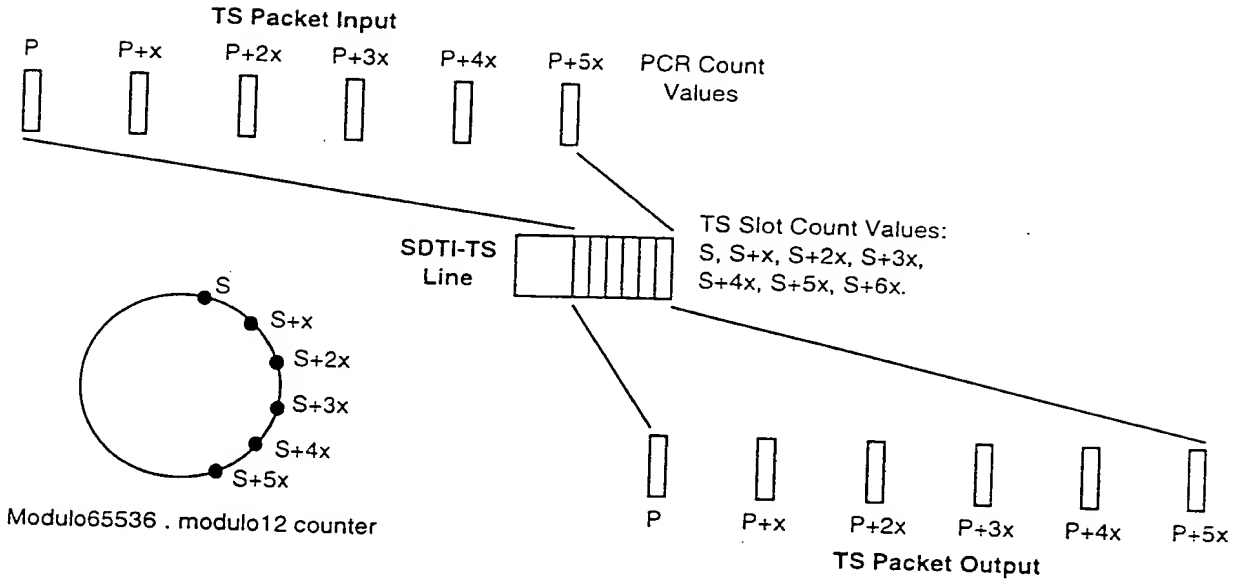

Figure 5: SDTI-TS Timing Reconstruction

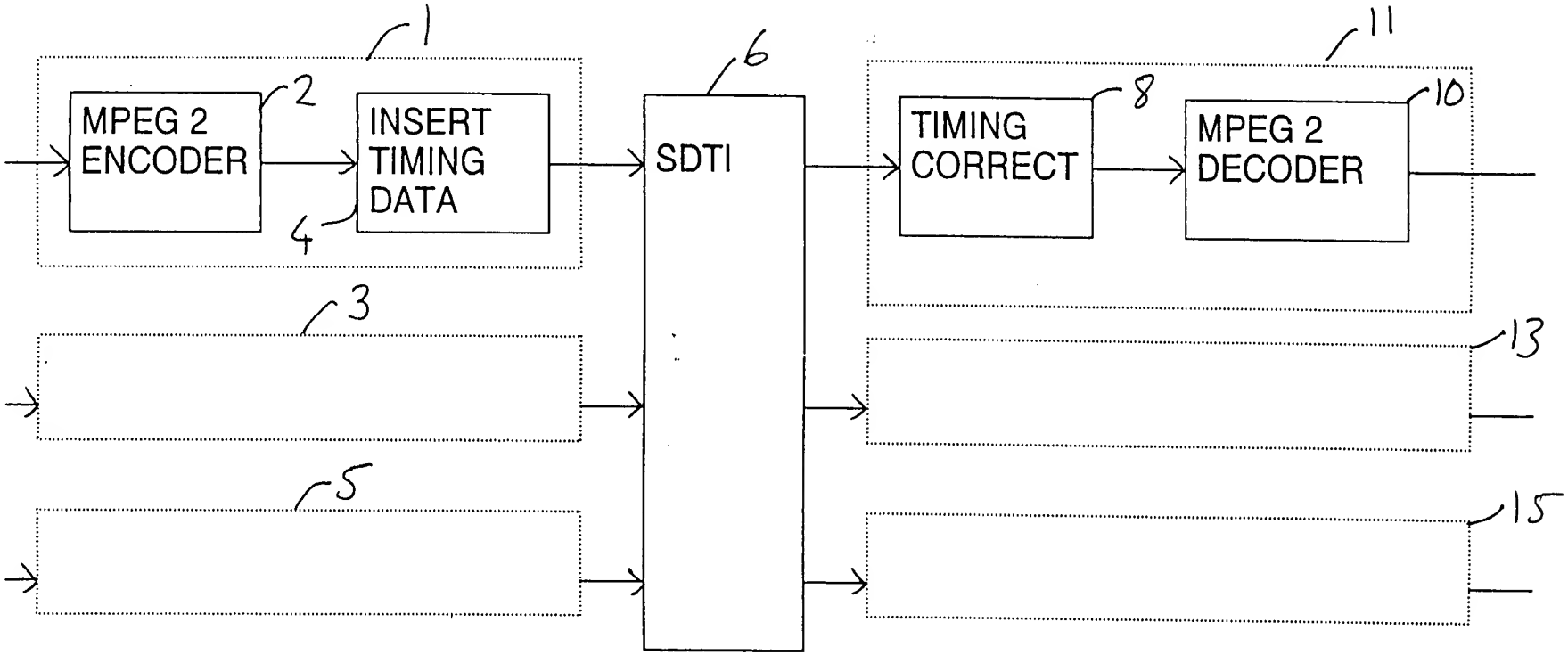

FIGURE 6

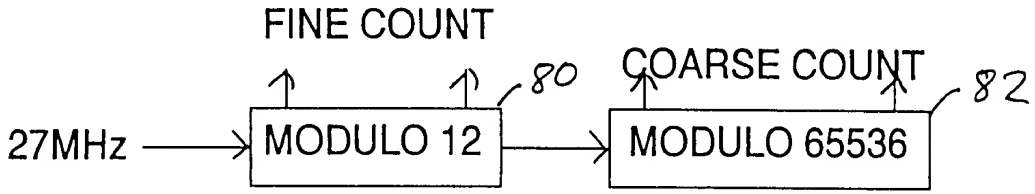

FIGURE 8

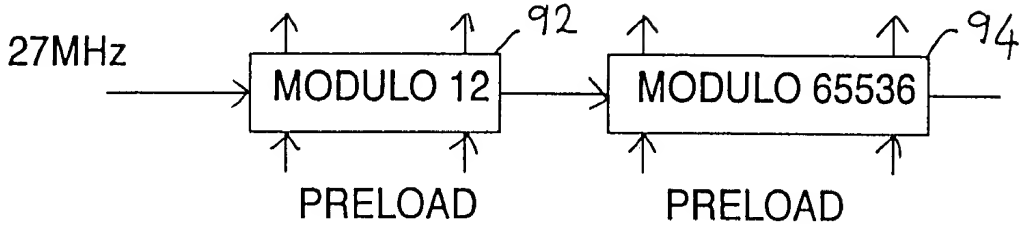

FIGURE 9

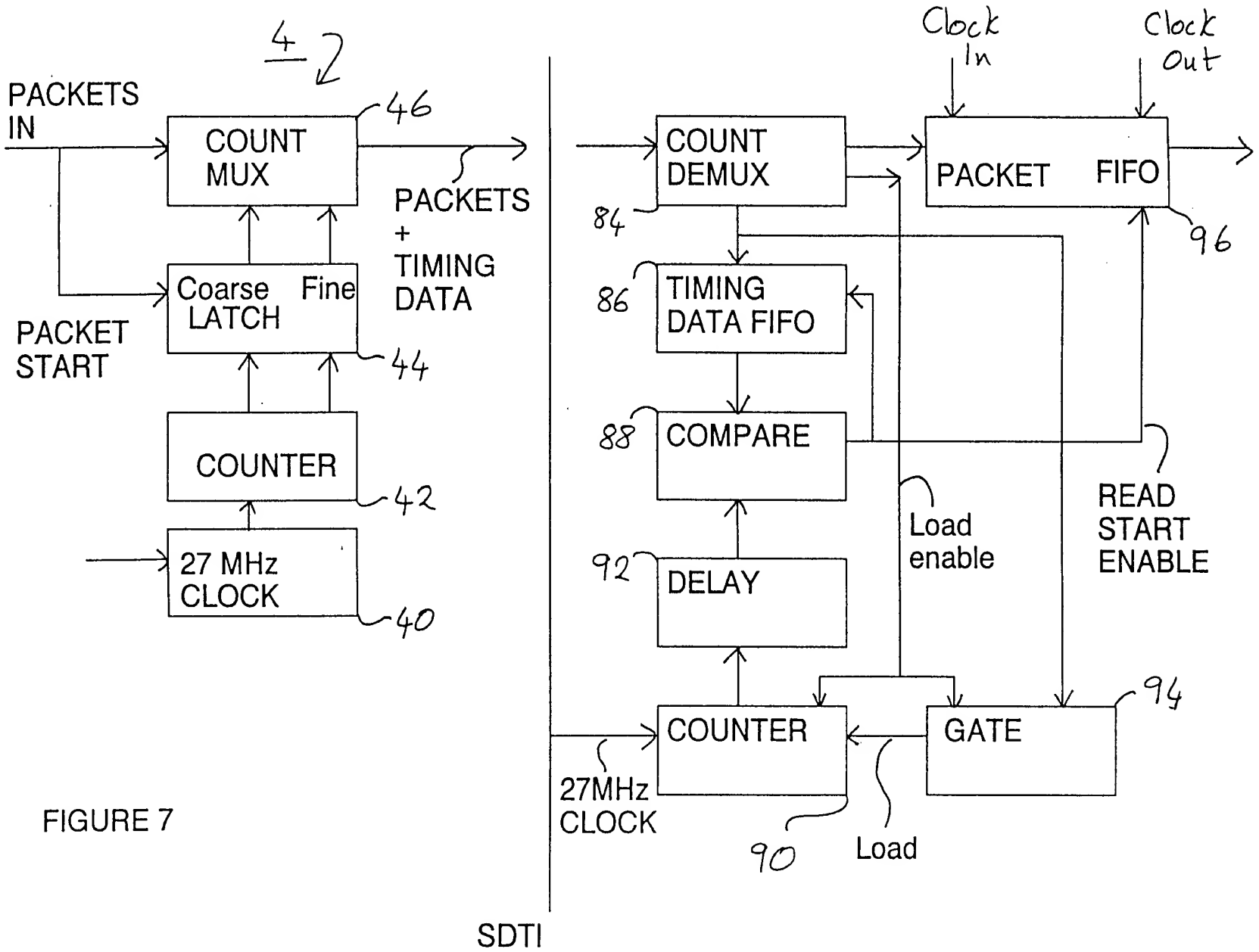
42
PACKETS IN
COUNT MUX
46
PACKETS + TIMING DATA
Coarse LATCH
Fine
PACKET START
44
COUNTER
42
27 MHz CLOCK
40
Clock In
Clock Out
COUNT DEMUX
84
PACKET FIFO
96
86
TIMING DATA FIFO
88
COMPARE
READ START ENABLE
Load enable
92
DELAY
94
COUNTER
GATE
27MHz CLOCK
90
Load
SDTI

FIGURE 7